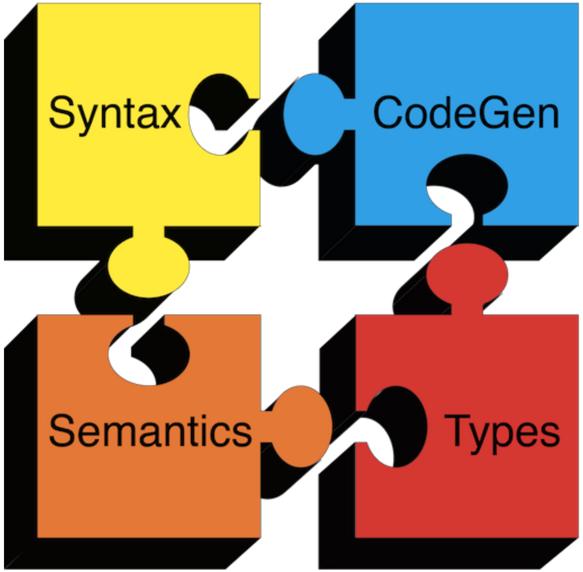
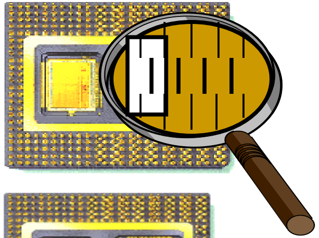
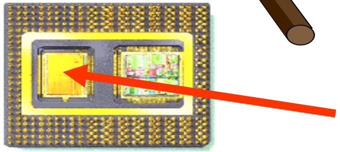


Compilers

Managing Caches

Alex Aiken

Managing Caches

	Registers	1 cycle	256-8000 bytes
	Cache	3 cycles	256k-1M
	Main memory	20-100 cycles	32M-4G
	Disk	0.5-5M cycles	4G-1T

Managing Caches

- Power usage limits
  - Size and speed of registers/caches
  - Speed of processors

- But
  - The cost of a cache miss is very high
  - Typically requires 2 caches to bridge fast processor with large main memory

- It is very important to:
  - Manage registers properly
  - Manage caches properly

Managing Caches

- Compilers are very good at managing registers
  - Much better than a programmer could be
- Compilers are not good at managing caches
  - This problem is still left to programmers
  - It is still an open question how much a compiler can do to improve cache performance
- Compilers can, and a few do, perform some cache optimizations

Managing Caches

- Consider the loop

```
for(j := 1; j < 10; j++)
    for(i=1; i<1000000; i++)
        a[i] *= b[i]
```

Managing Caches

- Consider the program:

```
for(i=1; i<1000000; i++)
  for(j := 1; j < 10; j++)
       a[i] *= b[i]
```

  – Computes the same thing
  – But with much better cache behavior
  – Might be more than 10x faster

- A compiler can perform this *loop interchange* optimization